DESIGNING w/ THE HMC414MS8G PA UTILIZING A LOW COST LAMINATED PRINTED CIRCUIT BOARD

General Description

The HMC414MS8G is a high efficiency GaAs InGaP Hetrojunction Bipolar Transistor (HBT) MMIC power amplifier, which operates between 2.2 - 2.8 GHz. The amplifier is packaged in a low cost, surface mount 8 lead package with an exposed base for improved RF and thermal performance. With a minimum of external components, the amplifier provides 20 dB of gain, +30 dBm of saturated power at 32 % PAE from a +5.0 V supply voltage. The amplifier can also operate with a 3.6 V supply. Vpd can be used for full power down or RF output power/current control.

Application Problem

An evaluation board from Hittite is provided in order to demonstrate the full performance of the HMC414MS8G power amplifier that uses Rogers high frequency laminate, RO4350. This laminate is specifically designed for RF/microwave circuits and displays stable properties over a broad range of environmental conditions. The board topology, shown in figure 1, is single layer with a ground plane height of 10 mils. The RF input and output circuitry is comprised of 50 Ω grounded coplanar transmission line with vias running along the transmission line to provide ground to the top metal. Although this design provides excellent performance at microwave frequencies, it may not be practical for many applications due to cost and level of integration. For this reason, board materials such as FR4, BT and GETEK are often used due to their low cost and multilayer properties. Grounded coplanar transmission lines also present a problem due to the requirement of ground vias along the line. In many multilayer boards, these vias would occupy valuable real estate, which is better suited for components. In order to address these issues, Hittite has designed an evaluation board utilizing a single layer FR4 board with microstrip line used as the transmission line topology. Although not multilayer, this design procedure can easily be adopted for many board topologies and materials. This product note will discuss the methodology used in the design.

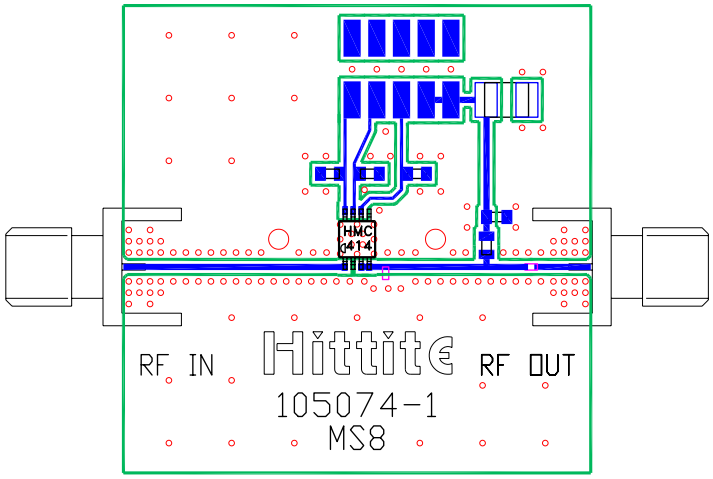

Figure 1 - HMC414MS8G evaluation board

Evaluation Circuit Composition

The HMC414MS8G evaluation board uses grounded coplanar transmission line for the RF input and output. The difference between grounded coplanar and microstrip is the distribution of the electric field. Figure 2 shows a comparison of the electrical field distribution between grounded coplanar and microstrip. The electric field lines in grounded coplanar are confined mainly between the transmission line and top layer ground although some of the field is distributed to the lower ground plane. In microstrip, the majority of the field is confined between the transmission line and ground with fringing fields off to the side. It is this field distribution which affects the impedance of the transmission line. Since the majority of the field in grounded

DESIGNING w/ THE HMC414MS8G PA UTILIZING A LOW COST LAMINATED PRINTED CIRCUIT BOARD

coplanar is coupled across the slot, it is the width of the slot that sets the impedance. This allows for the width of the transmission line to be either wide or thin, depending on the particular application. This is not the case in microstrip where width of transmission line is dictated by the dielectric constant and substrate height.

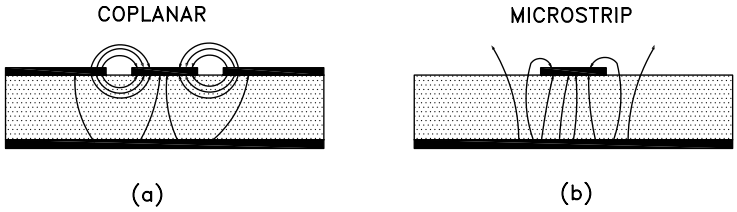

Figure 2 - (a) Grounded coplanar transmission line, (b) Microstrip transmission line

In order to demonstrate these differences, the line width, impedance of the grounded coplanar, and microstrip lines are calculated using a transmission line synthesizer tool, TLINE[1]. The board material is FR4 at a height of 62 mil and a ε_r=5.4. For a 50 Ω line impedance, a grounded coplanar line could be realized with a 6-mil gap and a 21-mil transmission line or a 9-mil gap and a 33 mil transmission line. A 50-Ω microstrip line on the same material requires a 113-mil transmission line width. This line width is excessive and presents a problem in most board layouts when interfacing to the amplifier I.C. Reducing the line width, from 113 mil to 35 mil (a more manageable width), increases the impedance from 50 Ω to 82 Ω. This increased impedance will affect the performance of the amplifier and mismatch the system. If microstrip line is to be used, the board height of the FR4 must be reduced or external circuitry must be added to transform the impedance back to 50 Ω. In this application, simple lowpass matching networks are used to transform the impedance.

Via holes are used in Printed Circuit Boards (PCB) to provide both RF and DC ground. While the ideal via is a perfect ground, the physical via contains parasitic inductance, resistance and capacitance to ground as shown in figure 3.

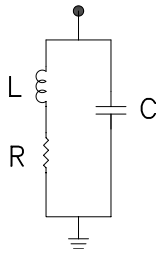

Figure 3 - Physical via model

The parasitic capacitance is the parallel plate capacitance of the via pad and the ground plane and is approximated by the equation:

$$C = \frac{A \cdot \varepsilon_r \cdot \varepsilon_o}{D}(F/m)$$

A=area of top pad

ε_o=permittivity of free space ($8.85*10^{-12}$ Farads/meter)

ε_r= relative permittivity

D= distance from via pad to ground plane

DESIGNING w/ THE HMC414MS8G PA UTILIZING A LOW COST LAMINATED PRINTED CIRCUIT BOARD

This capacitance is relatively low (< 0.05 pF) and, coupled with the operating frequency, will not dominate in the overall reactance of the via. However, the inductance and the resistance are factors in high power applications. The following equation can be used to estimate the via inductance[2]:

$$Lvia = \frac{\mu_0}{2\pi} \cdot \left[h \cdot \ln\left(\frac{h + \sqrt{r^2 + h^2}}{r} \right) + \frac{3}{2} \cdot \left(r - \sqrt{r^2 + h^2} \right) \right]$$

Where r is the radius of the via and h is the substrate height. From the equation it can be seen that as the height of the substrate increase so does the via inductance. Using the above equation the inductance of the 62-mil FR4 board and the 10 mil Rogers 4350 board is calculated. The calculated inductance for the Rogers 4350 is approximately, 0.016 nH, where the FR4 inductance is 0.43 nH. In addition, the resistance is higher in the FR4 board via since DC resistance is directly related to the length. DC resistance is calculated by the equation:

$$R = \frac{h}{\sigma A}$$

where h is the length of the via, A is the cross sectional area, and σ is the electrical conductivity of the metal.

The increased parasitics must be compensated for when laying out the circuit for the FR4 board. The overall inductance and resistance is reduced by using multiple vias in close proximity to all of the shunt components.

Designing The Output Matching Network From A Known Load

Typically, matching networks for power amplifiers are designed using load pull data measured from a particular amplifier or device. However, many times, this data is either not available or difficult to obtain due lack of equipment or time. Hittite has tuned the output matching networks to its power amplifiers for maximum output power and efficiency. Using these known load impedances, it is possible to design an equivalent matching network using different circuit topologies or board materials. Figure 4 shows the output load portion of the HMC414MS8G evaluation board. The output connector is terminated in a 50-Ω load and the device is removed to allow probing of the output-matching network. By placing the probe as close to the device output pin reference plane and ground plane as possible (see figure 4), the probe will be positioned to achieve the best ground-signal-ground as possible.

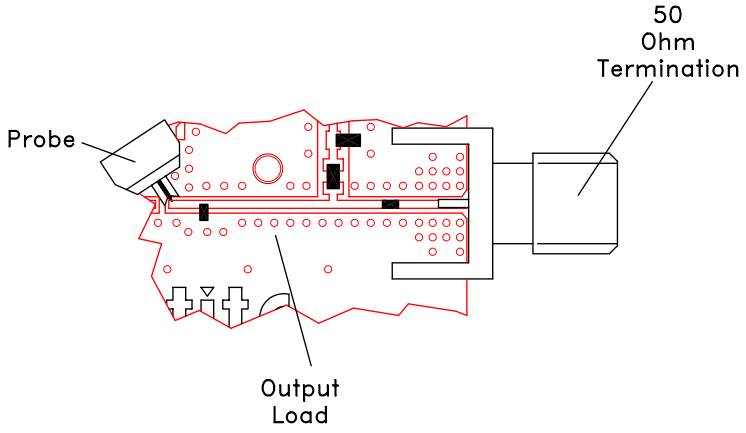

Figure 4 - HMC414MS8G evaluation board output load probe.

The probe is calibrated for a one-port measurement using calibration standards provided by the probe

DESIGNING w/ THE HMC414MS8G PA UTILIZING A LOW COST LAMINATED PRINTED CIRCUIT BOARD

manufacturer. The output load measurement is shown in Figure 5.

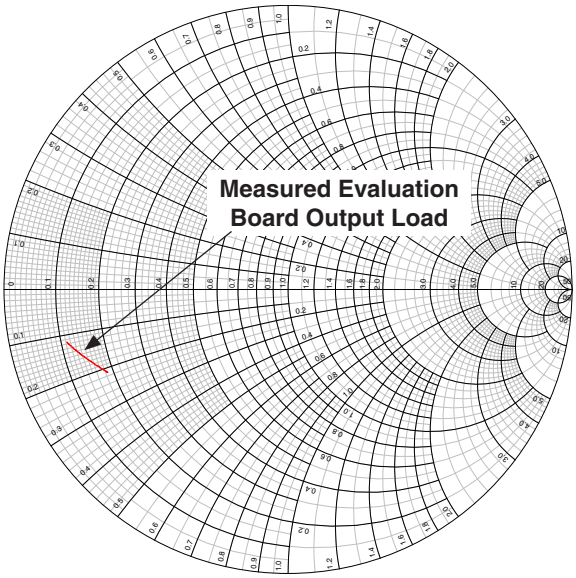

Figure 5 - Measured output load of HMC414MS8G evaluation board

Table 1 lists the impedance of the load at three frequency points. Notice that the resistance is less than 10 Ω . This is a typical optimum load match for a power amplifier. Depending on the periphery of the output device, the optimum load match is anywhere from 5 Ω to 20 Ω.

Frequency (GHz)	Resistance (Real Ω)	Reactance (Imaginary Ω)
2.2	9.3	-10.6
2.4	8.0	-8.9
2.8	5.6	-5.8

Table 1 - Measured output load impedance of HMC414MS8G evaluation board

HMC414MS8G FR4 Evaluation Board

FR4 board material is widely used throughout the industry in many consumer products because of its low cost and multilayer capabilities. Because of its wide popularity, many companies are manufacturing FR4 material. As a result, there is a large disparity in electrical properties owing to the wide range of manufacturing processes between the companies. In addition, to maintain cost, the manufacturing process is not held to a tight tolerance resulting in variations in loss tangent and dielectric constants. These variations are noticeable above 3 GHz and are the reason why FR4 is seldom used beyond this frequency. When performing a design using FR4 material it is essential to know the manufacturer and the electrical properties for the material being used. If the source of the board material is unknown by the board manufacturing house, then a specific board manufacturer should be requested. This request will avoid future difficulties during testing. For this design, the specifications for the board material was requested and received. The critical parameters are listed in table 2.

DESIGNING w/ THE HMC414MS8G PA UTILIZING A LOW COST LAMINATED PRINTED CIRCUIT BOARD

FR4 Material Critical Parameters		
Parameter	Specification	Units
Height (h)	62	mil
Permittivity (ε_r)	5.4	--
Loss Tangent (δ)	0.035	--
Copper Thickness (T)	1.4	mil

Table 2 - Critical FR4 board material specifications

Design of Output Matching Network

Using the data obtained from the probing of the output load of the HMC414MS8G evaluation board, a matching network for the FR4 board is designed. Initially an ideal matching network will be designed to determine roughly the required inductance and capacitance. From Figure 5, it can be seen that a low pass network will be adequate to match the 50 Ω output to the desired load impedance. Starting from 50 Ω, a shunt capacitor will rotate along the constant admittance line intersecting the constant impedance line where the output load is located. A series inductance is then required to move up the constant impedance line. To simplify the process, a matching synthesis program is used to match a single frequency point from Table 1.[4] The initial synthesis yielded a result that has higher inductance than required. Reducing the series inductor produced the results in Figure 6.

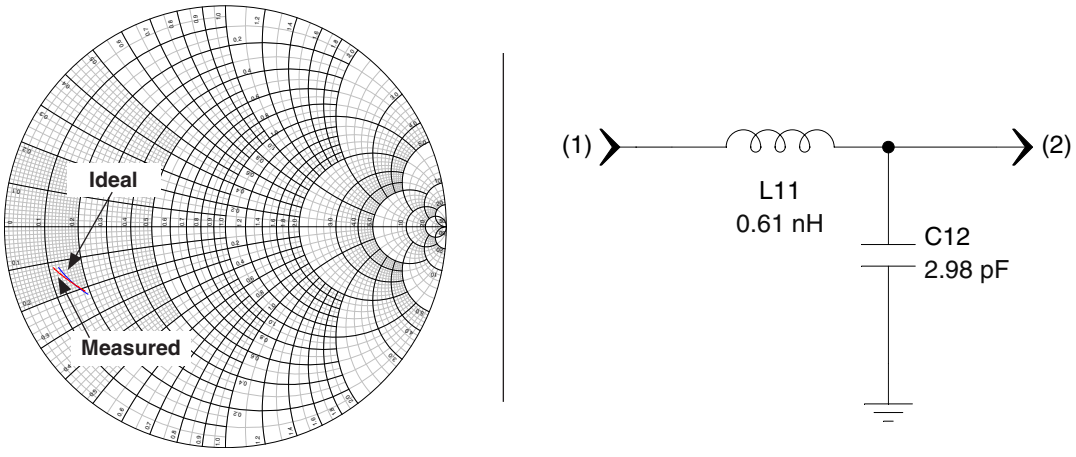

Figure 6 - **(a)** Measured load data versus ideal, **(b)** Ideal matching network

Using the topology from the ideal matching network the final matching network is designed using the FR4 material previously described. The layout for the entire FR4 board is shown in Figure 7, which also includes an input-matching network.

DESIGNING w/ THE HMC414MS8G PA UTILIZING A LOW COST LAMINATED PRINTED CIRCUIT BOARD

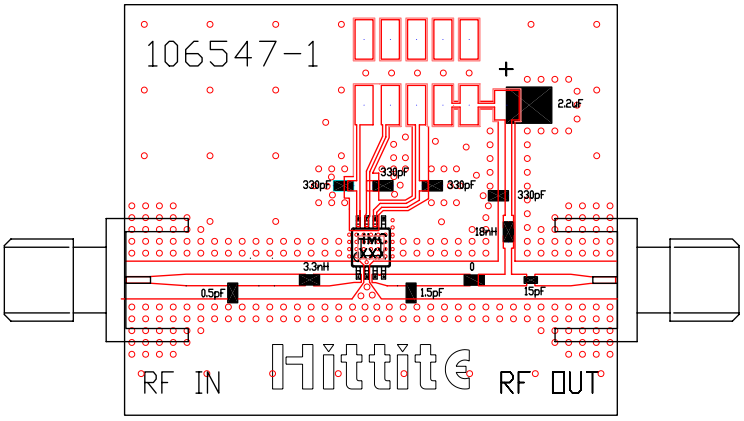

Figure 7 - The HMC414MS8G FR4 evaluation board

Ideally, the RF traces into and out of the amplifier are 50 Ω. However, in this case, a 50 Ω line would be too wide (113 mil). For this application, a more manageable line width is 35 mil, which has an impedance of 87 Ω. The high impedance line is used as a series inductor on the output-matching network. After tuning, the value of the shunt capacitor is reduced to 1.5 pF. A 15-pF series blocking capacitor and an 18 nH choke is added for DC bias. The capacitors used in the matching network are high Q microwave ceramic capacitors. It is important to insure that the equivalent series resistance (ESR) of the capacitors is low to minimize loss. The capacitors should always be operated below or at the series resonance. Above series resonance, the reactance is inductive. In addition, the parallel resonance's should be calculated to insure that they do not fall in the band of operation. The above output matching was simulated using Eagleware's Genesys[5] basic simulation software. S-parameter files from the capacitor and inductor vendors are used in the simulation file to improve the accuracy of the model. The results of the simulation are compared to the probed output load of the original evaluation board. As shown in Figure 8, there is good agreement between the simulated and actual load data.

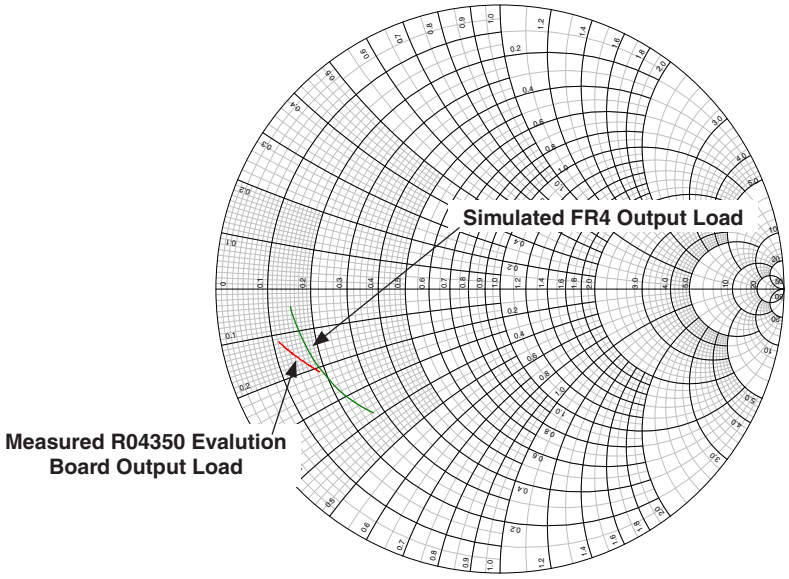

Figure 8 - Measured versus simulated output load

For price, delivery, and to place orders, please contact Hittite Microwave Corporation:
12 Elizabeth Drive, Chelmsford, MA 01824 Phone: 978-250-3343 Fax: 978-250-3373
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DESIGNING w/ THE HMC414MS8G PA UTILIZING A LOW COST LAMINATED PRINTED CIRCUIT BOARD

Design of Input Matching Network

Normally, the HMC414MS8G power amplifier input is adequately matched. However, since high impedance lines are being used, the input match is slightly degraded. To improve the input match, a low pass matching network is used.

As with the output-matching network, an ideal input matching network is synthesized to establish a baseline for the component values. The input impedance is determined with the output-matching network in place. To shift the reference plane from the input of the evaluation board to the reference plane of the amplifier, an electrical delay is applied to the network analyzer. The amount of delay was determined by placing a short at the input reference plane of the amplifier (See Figure 9). A measurement was taken using an HP8753D Network Analyzer. A matching network is then synthesized to match 34.6-j24.9 Ω to 50 Ω.

A matching synthesis program is utilized to determine the optimum input matching network for a frequency range of 2.2 GHz to 2.8 GHz. The ideal input matching network consists of a shunt 0.9-pF capacitor and a series 3.3 nH inductor. Figure 10 (a) shows the simulated input match versus the input match with no matching network.

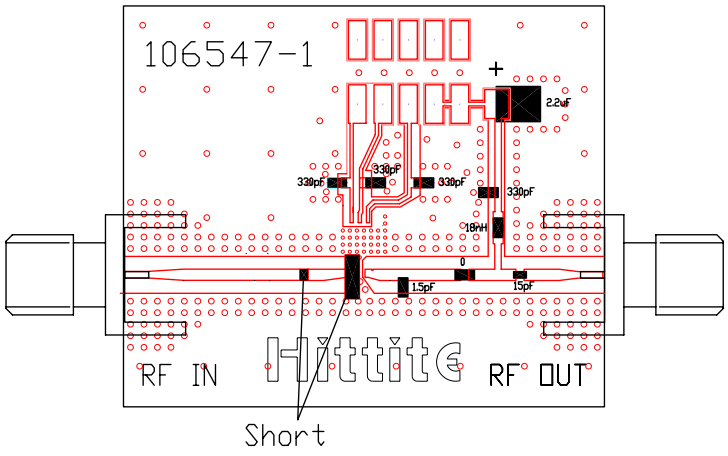

Figure 9 - Determining the reference plane of the input

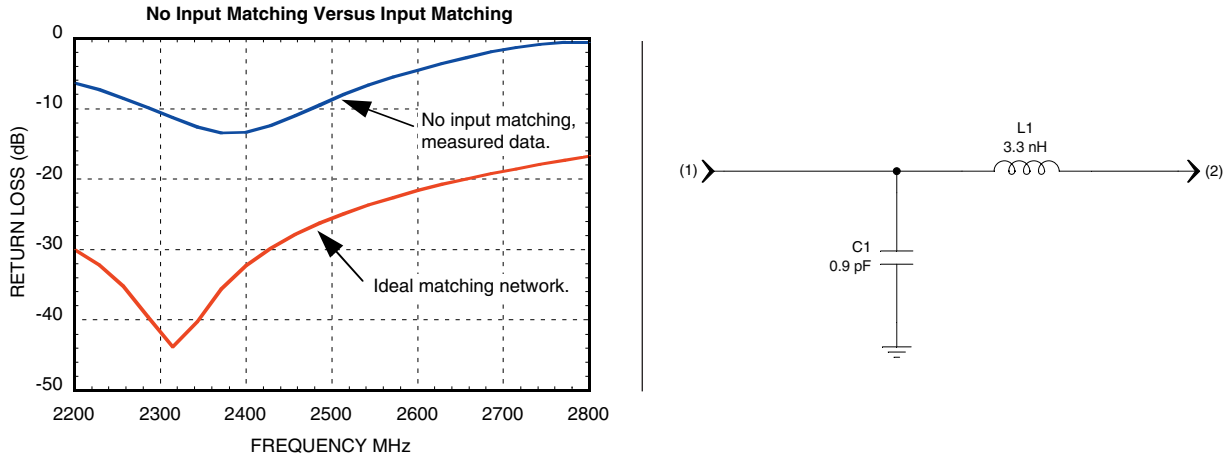

Figure 10 - (a) Matched input versus non matched input, (b) Ideal input matching network

DESIGNING w/ THE HMC414MS8G PA UTILIZING A LOW COST LAMINATED PRINTED CIRCUIT BOARD

Figure 7 shows the input match as it is implemented on the FR4 board. During test, it was determined that the optimum value for the shunt capacitor is 0.5 pF instead of 0.9 pF. The value of the inductor remained the same.

The HMC414MS8G power amplifier input is in line with its output separated by a single pin. Unless the pin is properly grounded, feedback from the output will cause the amplifier to oscillate. Figure 11 shows pin 2 well grounded with the ground plane tapering up to the pin. This will provide the necessary isolation between the input and output to prevent potential oscillations.

Measured Results

The board was measured for gain, return loss, 1 dB compression, saturated output power and efficiency. These measured results are shown in figures 12,13,14 and 15, respectively. The results are compared to HMC414MS8G evaluation board, which is constructed on Rogers 4350 high frequency laminate. Bias voltage is set to 3.6 V resulting in a quiescent current of approximately 240 mA.

In order to accurately assess the performance of the circuit, the losses from the transmission line and connectors are de-embedded from the initial measured results. These losses are calculated up to, but not including the matching networks. Figure 11 shows the reference planes from which the losses are calculated.

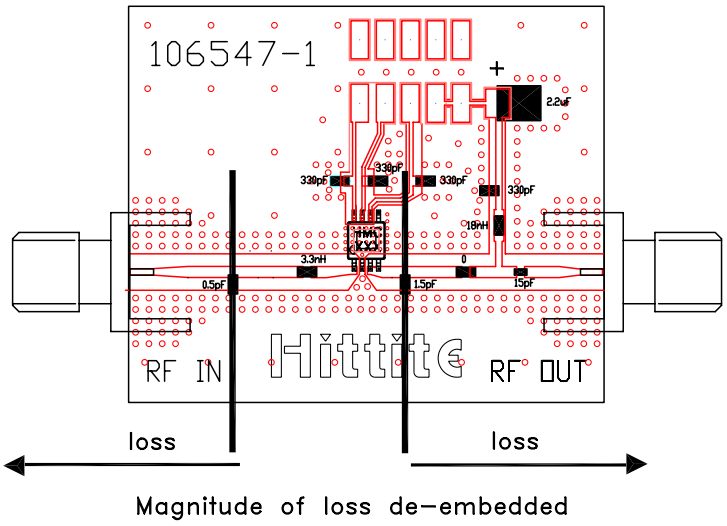

Figure 11 - Reference planes of calculated board loss

A simplified model of the connector is used to determine its losses. The simple model consists of a length of coaxial line, which is dimensionally equivalent to the connector. The losses due to the transmission line are calculated using =EMPOWER=[6], an electro-magnetic simulator. Table 3 lists the magnitude of the losses. Notice that the output loss does not increase with higher frequency. This is due to the bias choke, which has a higher reactance at the upper frequencies.

Board Loss			
Frequency (GHz)	Input Loss (dB)	Output Loss (dB)	Total Loss (dB)
2.2	0.53	1.00	1.53
2.4	0.58	1.00	1.59
2.8	0.72	0.92	1.65

Table 3 - Simulated board losses

DESIGNING w/ THE HMC414MS8G PA UTILIZING A LOW COST LAMINATED PRINTED CIRCUIT BOARD

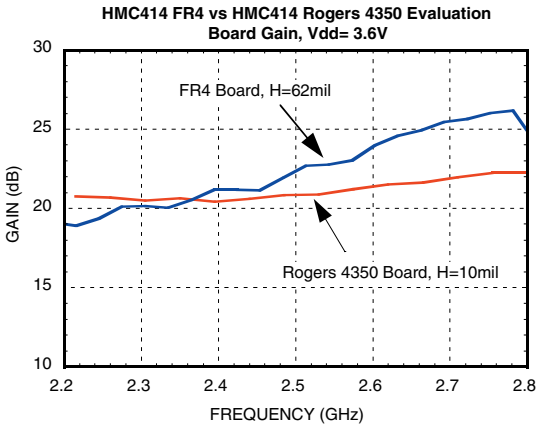

Figure 12 - Gain, FR4 board versus HMC414MS8G evaluation board

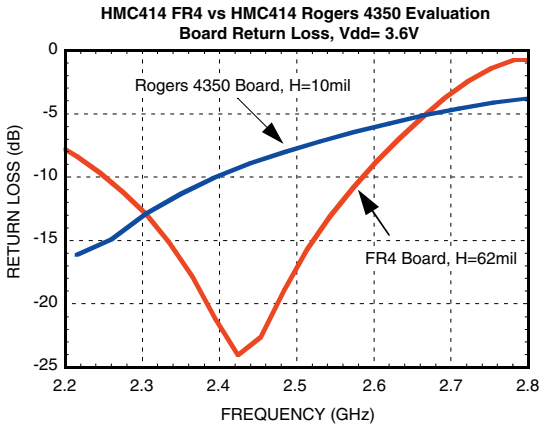

Figure 13 - Return loss, FR4 versus HMC414MS8G evaluation board

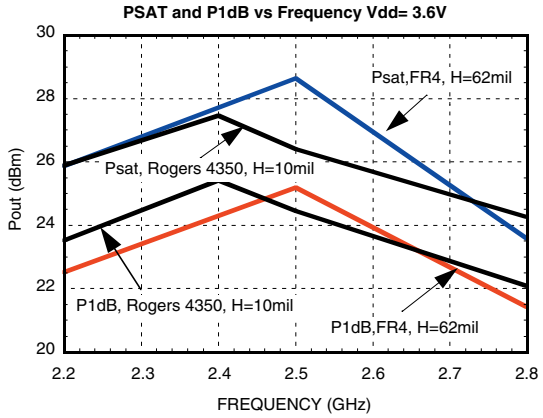

Figure 14 - P1dB and saturated power, FR4 versus HMC414MS8G evaluation board

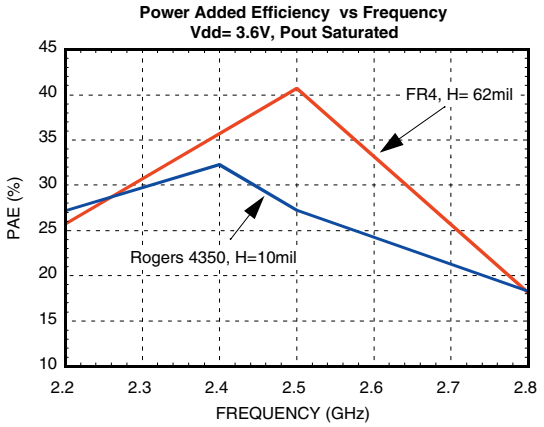

Figure 15 - Power Added Efficiency (PAE), FR4 versus HMC414MS8G evaluation board

Table 4 lists the specifications for the HMC414MS8G power amplifier as set in the Hittite data sheet. Comparing the measured results to the table shows that the FR4 board design meets or exceeds the minimum requirements.

Parameter	Vdd= 3.6V			Units
	Min. Spec / FR4	Typ.	Max. Spec / FR4	
Frequency Range	2.2-2.8			GHz
Gain	17 / 19	20	25 / 26	dB
Input Return Loss	3 / 3[1]	8	-- / 24	dB
Output Power for 1dB Compression (P1dB)	21 / 21.5	25	-- / 25	dBm
Saturated Output Power (Psat)	23 / 23.5	27	-- / 28	dBm
Supply Current (Icc) Vpd=3.6V	240 / 240	--	--	mA
Notes: Minimum occurs at 2.7GHz				

Table 4 - Electrical specifications, Ta=+25° C, Vpd=3.6V

DESIGNING w/ THE HMC414MS8G PA UTILIZING A LOW COST LAMINATED PRINTED CIRCUIT BOARD

Thermal Considerations and Analysis

One parameter that is often overlooked in amplifier design is thermal relief. Many times a part will be designed with excellent initial performance only to fail later due to excessive temperature. These failures can be avoided by following a few simple steps. Figure 16(a) shows a transparency of the HMC414MS8G in its MS8G package. Beneath the package, there are several vias with a diameter of 15 mils. It is best to have additional smaller vias under the package instead of fewer larger vias. Smaller vias are more easily filled with solder (less voids) allowing for a more efficient transfer of heat. In addition, thermal resistance from the flange to ground is inversely proportional to the number of vias.

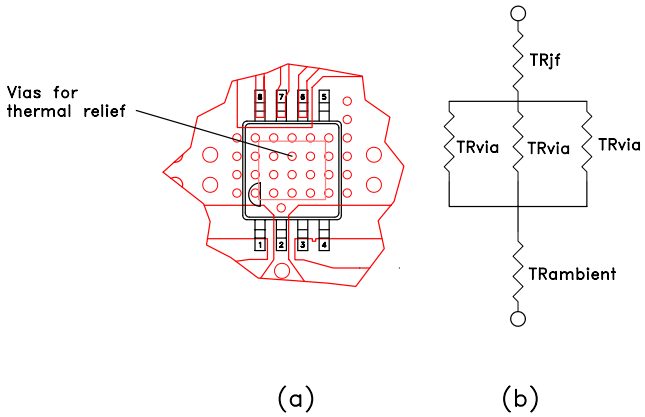

Figure-16 - (a) Via hole placement beneath flange, (b) simplified thermal model

Figure 16(b) shows a simple thermal model of a part mounted on a board. It consists mainly of three thermal resistances, from the junction to the flange (TRjf), the flange to the bottom of the board (TRvia), and from the bottom of the board to air (Trambient). The thermal resistance from the junction to the flange is typically supplied by the manufacturer and in the case of the HMC414MS8G, it is 37 °C/W at a maximum flange temperature of 85 °C. Trambient is a function of copper thickness, surface area, and surface radiation. Determination of TRambient is a complicated process and therefore beyond the scope of this application note. However, the thermal resistance of the via is approximated with the following equation:

$$TRvia = \frac{h}{\sigma \cdot \pi \cdot (R_{outer}^{2} - R_{inner}^{2})}$$

Where, h=length of the via (cm), σ =thermal conductivity of the via metal (W/cm-K), R_{outer}=outer radii of the via (cm), and R_{inner}=the inner radius of the via (cm). From the equation, two observations are made; 1) longer vias have higher resistance and 2) filled vias have lower resistance than open vias. It is the latter observation which highlights the benefits of filling the vias with solder. Finally, the number of vias will decrease the resistance by 1/N, where N is the number of vias. An example is in order to demonstrate the application of the above equations.

Example:

It was previously mentioned that the thermal resistance of the HMC414MS8G is 37 °C/W. This information is extracted from the Hittite data sheet for this particular part. However, this information may not be obvious and, as a result, warrants further explanation. The information supplied in the data sheet is in the form of absolute ratings. The maximum channel temperature (junction temperature) for this device is 150 °C for a continuous power dissipation of 1.73 W at a flange temperature of 85 °C. From this information the thermal

resistance is calculated using the following equation:

$$TR_{jf} = \frac{T_{junction} - T_{flange}}{P_{disssipated}}$$

Using the information presented in the data sheet results in a thermal resistance of 37 °C/W. The same information can also be extracted by taking the inverse of the thermal conductance, which is also given in the absolute maximum ratings section of the data sheet. For the HMC414MS8G the thermal conductance is 27 mW / °C (Note: the thermal conductance in the data sheet is referred to as a "de-rating factor").

Using the equation to calculate the via thermal resistance, the thermal resistance is computed to be 152 Ω. This resistance is calculated for a via that is 0.062 " long with a diameter of 0.015 " and is filled with solder. Figure 16(a), shows that nine vias reside directly under the package flange. These vias will contribute to the majority of the heat transfer from the bottom of the package to the bottom of the board and are included in the model. The heat transfer contribution of the remaining vias is complex and will not be included in the model. The nine vias will reduce the thermal resistance of the via by 1/9 to 17 Ω.

In order to establish a reference temperature, a probe is placed on the bottom of the board directly below the package flange. The amplifier is biased with 5 V with an input power of 15 dBm. The output power is 30 dBm with a DC current of 432 mA. The amplifier is left on until the temperature at the bottom of the board reaches steady state. The temperature is observed to be 63.8 °C with a surrounding ambient temperature of 27 °C. The amount of power dissipated as heat is calculated using the following equation:

$$P_{dissipated} = V_{DC} \cdot I_{DC} + P_{in} - P_{out}$$

A model for the HMC414MS8G mounted on the FR4 board is shown in Figure 17. The thermal resistance from the back of the board to the surrounding air has been omitted since the temperature of the board was allowed to reach steady state. The model is comprised of a constant current source, which is representative of the dissipated power and the thermal resistance of the junction to flange (TR_{jf}), and from the flange to the bottom of the board (TR_{via}).

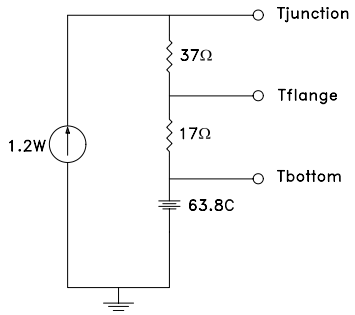

Figure 17 - The HMC414MS8G amplifier on FR4 board, simplified thermal model

This simplified thermal model is analyzed in the same way a simple electronic circuit is analyzed by using either Ohm's or Kirchoff's laws. For example, to determine the temperature of the flange

The following equation is used:

$$T_{flange} = TR_{via} \cdot P_{dissipated} + T_{bottom}$$

DESIGNING w/ THE HMC414MS8G PA UTILIZING A LOW COST LAMINATED PRINTED CIRCUIT BOARD

In this particular case, the flange temperature is determined to be 84.2 °C. Making the appropriate substitutions in the above equation yields a junction temperature of 128.6 °C. The analysis shows that the junction temperature of the device is below the critical threshold of 150 °C. However, this is at an ambient temperature of 27 °C which suggests that a heatsink would be required if the device is to be operated at higher ambient temperatures. Using the same procedure the maximum ambient temperature, before the junction exceeds 150 °C, is calculated to be approximately 49 °C.

The procedure and model used in the thermal analysis of the board should be used to establish baseline conditions only. Thermal analysis is complex with many variables that will affect the outcome. Upon establishing a baseline, a thorough thermal analysis should be performed to determine the optimum board design.

Conclusion

A power amplifier that originally was mounted and tuned on high frequency laminate is mounted on low cost FR4 board utilizing high impedance microstrip lines. Using sound RF practices, a low pass output-matching network is designed that presents the optimum load to the power amplifier. In addition, a low pass matching network is synthesized that transforms the high impedance line at the input to the input load impedance of the amplifier. A simple thermal analysis is performed which shows how to translate the measured temperatures at the bottom of the PC board to the junction of the device. The techniques in this product note can be extended to other Hittite power amplifiers by using load and temperature data provided by Hittite Microwave Corporation.

(Endnotes)

[1] =TLINE=, transmission line synthesizer software, Eagleware Corporation

[2] Arbie, Peter, L.D., “Design of RF and Microwave Amplifiers and Oscillators”, Norwood, MA: Artech House, 1999

[4] =Match=, matching network synthesizer software, Eagleware Corporation

[5] Genesys V8, RF and Microwave linear simulation software, Eagleware Corporation

[6] =EMPOWER=, electromagnetic simulation software, Eagleware Corporation